IN THE CLAIMS

Please amend the claims to read as follows:

Please cancel claims 1, 7 and 20 without prejudice.

Claim 1 (canceled)

Claim 2 (currently amended) The method of claim [[1]] 21 wherein [[the]] said SOI layer is thinned by successive oxidation and stripping steps forming a thinned SOI layer.

Claim 3 (currently amended): The method of claim 2 wherein a pad oxide and a pad nitride layer are formed over [[the]] said thinned SOI layer prior to forming said isolation trench.

Claim 4 (currently amended): The method of claim 3 ~~wherein an~~ including:

stripping said pad oxide and said pad nitride after said isolation trench is formed in [[the]] said device, and ~~separating the thinned SOI layer into first and second regions~~

then forming a sacrificial oxide layer over said N and P ground plane regions prior to doping said N and P ground plane regions; and

then stripping said sacrificial oxide layer.

Claim 5 (currently amended): The method of claim 21 [[,4]] wherein an isolation dielectric is formed filling the isolation trench prior to doping said N and P wells.

Claim 6 (currently amended): The method of claim 5 wherein [[the]] said N and P wells ~~first and second regions~~ are ion implanted with N-type dopant and P-type dopant to form an SOI N-well and an SOI P-well respectively prior to forming said semiconductor channel regions directly on said N and P wells.

Claim 7 (canceled).

Claim 8 (currently amended): The method of claim [[7]] 21 wherein in situ counter doping is provided in the epitaxial layers.

Claim 9 (previously presented): The method of claim 8 wherein a liner is formed in the isolation trench prior to forming the isolation dielectric.

Claim 10 (previously presented): The method of claim 8 wherein a sacrificial layer is applied before forming the N-well and the P-well and is stripped away thereafter.

Claim 11 (currently amended): A [[The]] method of ~~claim 1 including the step of~~ manufacture of a Super Steep Retrograde Well (SSRW) FET (Field Effect Transistor) device comprising:

forming an SOI layer on a substrate;

thinning said SOI layer to form an ultra-thin SOI layer;

forming an isolation trench separating said SOI layer into N and P wells and ground plane regions;

doping the N and P wells and ground plane regions formed from said SOI layer with N-type and P- type dopant respectively;

forming intrinsic semiconductor channel regions above said N and P wells and ground plane regions;

forming gate electrode stacks above said channel regions and forming FET source and drain regions; and

forming a diffusion retarding barrier in the surface of [[the]] said N and P wells and ground plane regions. ~~ground plane regions.~~

Claim 12 (previously presented): The method of claim 11 wherein the SOI substrate is thinned by successive oxidation and stripping steps forming a thinned SOI layer.

Claim 13 (currently amended): The method of claim 12 wherein a pad oxide and a pad nitride layer are formed over [[the]] said thinned SOI layer.

Claim 14 (currently amended): The method of claim 13 wherein an isolation trench is formed in the device separating [[the]] said thinned SOI layer into first and second regions.

Claim 15 (currently amended): The method of claim 14 wherein an isolation dielectric is formed filling [[the]] said isolation trench.

Claim 16 (previously presented): The method of claim 15 wherein the first and second regions are ion implanted with N-type dopant and P-type dopant to form an SOI N-well and an SOI P-well respectively.

Claim 17 (currently amended): The method of claim 16 wherein an intrinsic epitaxial layers are [[is]] formed with an intrinsic epitaxial layer above each of [[the]] said SOI N-well and [[the]] said SOI P-well respectively.

Claim 18 (currently amended): The method of claim 17 wherein in situ counter doping is provided in [[the]] said intrinsic epitaxial layer[[s]].

Claim 19 (currently amended): The method of claim 18 wherein:

a liner is formed in [[the]] said isolation trench prior to forming [[the]] said isolation dielectric;

a sacrificial layer is applied before forming [[the]] said N-well [[;]] and [[the]] said P-well and is said sacrificial layer is stripped away thereafter.

Claim 20 (canceled)

Claim 21 (new) A method of manufacture of a Super Steep Retrograde Well (SSRW) FET (Field Effect Transistor) device comprising:

forming an SOI layer on a substrate;

thinning said SOI layer to form an ultra-thin SOI layer;

forming an isolation trench separating said SOI layer into an N well and a P well including ground plane regions in said N well and in said P well, each of said N well and said P well having a top surface;

doping said N well and said P well formed in said SOI layer with N-type and P- type dopant respectively;

forming an epitaxial semiconductor layer on said top surfaces of said N well and said P well;

forming gate electrode stacks above said epitaxial semiconductor layer with channel regions therebelow; and

forming FET source regions and drain regions in said epitaxial layer and in both said N well and said P well.

Claim 22 (new) A Super Steep Retrograde Well (SSRW) FET (Field Effect Transistor) device comprising:

an ultra-thin SOI layer formed on a substrate;;

an isolation trench separating said SOI layer into a N type doped N well and a P type doped P well including ground plane regions in said N well and in said P well, each of said N well and said P well having a top surface;

an epitaxial semiconductor layer formed on said top surfaces of said N well and said P well;

gate electrode stacks formed above said epitaxial semiconductor layer with channel regions therebelow; and

FET source regions and drain regions formed in said epitaxial layer and in both said N well and said P well.

Claim 23 (new): The device of claim 22 wherein a diffusion retarding barrier is formed in the surface of said N and P wells and ground plane regions.